STRATEGIC MARKETS

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San Francisco — Decision roller derby: multiple paths down the Roadmap

Debra Vogler, Senior Technical Editor

A showcase for solutions has never been more in need now that divergent paths down the industry roadmap have evolved. The complexities of more metallization layers, integrating Cu/low-*k* interconnect structures, extending 248nm and now 193nm lithography, combined with rising chip design and mask set costs, have all set the stage for more indecision when planning the transition from 90nm to 65nm. Further upset has occurred because the business and technology requirements, combined with financial constraints, have forced low-volume players and those not in the high-end microprocessor segment into a "decision roller derby" of sorts. Manufacturing strategies — including what tools to buy and when — require re-tooling.

Lithography

The segment most affected by the decision roller derby is lithography. With as much certainty as one dares admit, it appears that 193nm lithography will be extended using immersion down to at least the 45nm node, if not lower (see **ASML**'s TWINSCAN XT:1400).

When 157nm happens, it will probably be more suited for low-volume applications, but what happens after that is not clear. One expert has suggested there may be a fundamental limit on resist chemistry — starting around 40–45nm — that prevents high-fidelity imaging, a mechanism not yet understood.

Another "hit" on lithography infrastructure comes from rising mask costs: "The main problem today is yield — if the maskmakers could write a functional mask once and ship it, they could survive at present price and volume levels," Marc Levenson, editor-in-chief of *SST* sister publication *Microlithography World*, has noted. Show attendees should keep their eyes open for products that target mask yield, as well as those that assist in reducing the impact of data volume "explosion," for example.

Transistor scaling

The debate on annealing technologies continues on several fronts. One strategy — using co-implants — will enable spike anneal to be used for at least one more generation, according to Susan Felch, program manager, USJ development at **Applied Materials**, thereby delaying the need to go to something new with the associated risks. Ion implant tools at the show include Applied Materials' Quantum X and **Tokyo Electron Limited**'s iStar.

No matter the ultimate solution, the replacement for conventional spike annealing will have lowered thermal budgets. Flash lamp (millisecond) annealing and sub-melt laser annealing hold promise, although both have technical shortcomings. SPER (solid-phase epitaxial regrowth) has to overcome integration issues and leakage-current challenges that come from residual defects after the process, but the ability to use existing process tools is a plus.

The path to high-k gate dielectrics appears a bit more predictable. John Borland, founder of **J.O.B. Technologies**, has predicted that medium-k ($k \approx 11–15$) will first be used at the 65nm node, followed by metal-gate electrodes at the 45nm node; high-k would be next — requiring metal-gate electrodes at the 45 to 32nm nodes. In the meantime, the industry will be looking for products that continue to target gate silicide technology (e.g., Applied Materials' Endura2).

Interconnect

Although chipmakers have reported success at integrating fragile low-k materials at the 90nm node, there is a simmering debate about their ability to survive successive processing steps — especially CMP and packaging. **The Dow Chemical Co.**'s SiLK Y is entering the fray with reduced closed-pore sizes.

Wafer cleaning/surface treatments

Changes in surface cleaning and treatments — such as single-wafer wet cleaning and supercritical carbon dioxide — are being forced by more stringent CMP process requirements, implementation of low-k films (and ULK), and advanced USJ technologies. **SCP Global Technologies**' Emersion 300 is an example of a single-wafer immersion cleaning tool that targets both FEOL and BEOL applications. **SEZ**'s Da Vinci series of single-wafer wet processing tools addresses the front and backside of wafers.

Metrology

The possibility of 193nm immersion lithography being able to meet performance once expected of 157nm technology, along with fast-approaching CD requirements for immersion, is going to have an impact on metrology and could accelerate the adoption of relatively novel techniques, such as scatterometry, in-line AFM, and wireless metrology. Integrated metrology is gaining momentum as fabs seek ways to save money and cleanroom space. Some of the many products coming out of this segment are: **KLA-Tencor**'s Surfscan SP2, **n&k Technology**'s 3300DR, **Nova Measuring Instruments**' NovaScan 3090, and **Rudolph Technologies**' WaferView defect inspection team.

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This year, *Solid State Technology* will sponsor the 2nd Annual Attendees' Choice Awards for Semicon West. Attendees of either or both the San Francisco (wafer processing) and San Jose (final manufacturing) shows can vote for the best products exhibited at each show in three separate categories:

- Best solution to a problem
- Most innovative product
- Best cost-of-ownership product

Ballots are available at *Solid State Technology*'s booth (#5953 in San Francisco, #11407 in San Jose). Only one vote per attendee is allowed. Completed ballots must be submitted at these booths prior to 5:00 pm on the second day of each show.

Winners in each category will be announced on the last day of each show.

All voters who identify themselves on their ballots will be eligible for a drawing that will determine the winner of a new smart phone. Eligible voters need not be present at the drawing to win; the winner will be contacted the week after Semicon West.

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Author(s) : Debra Vogler

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